BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

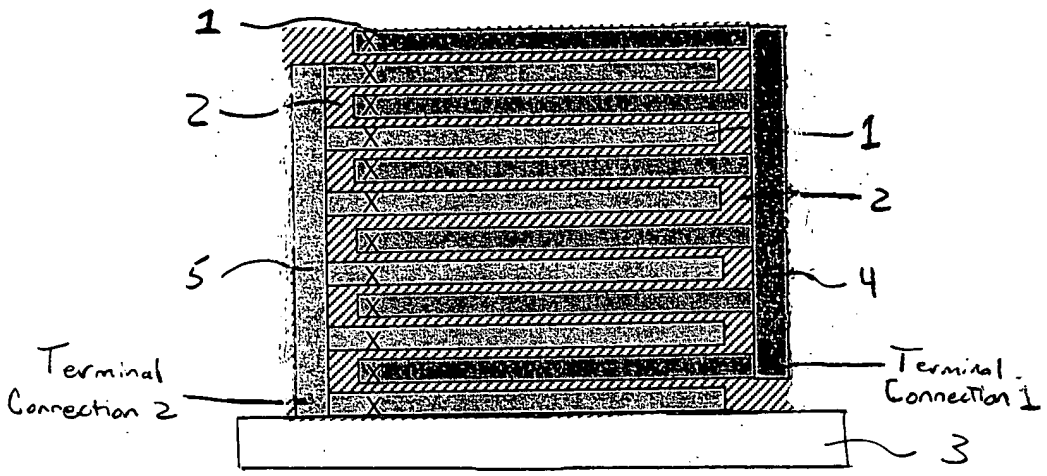
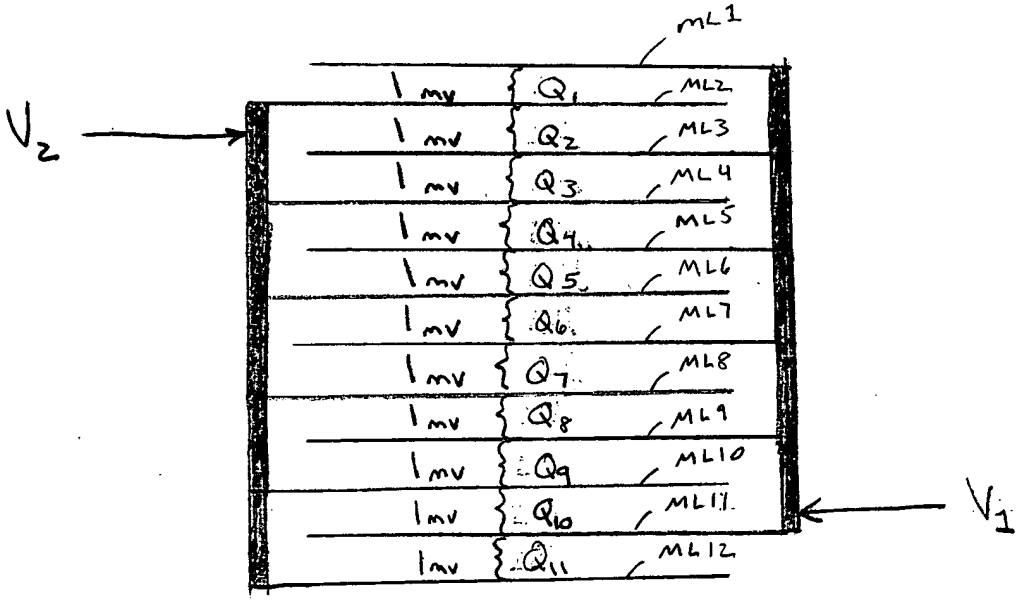


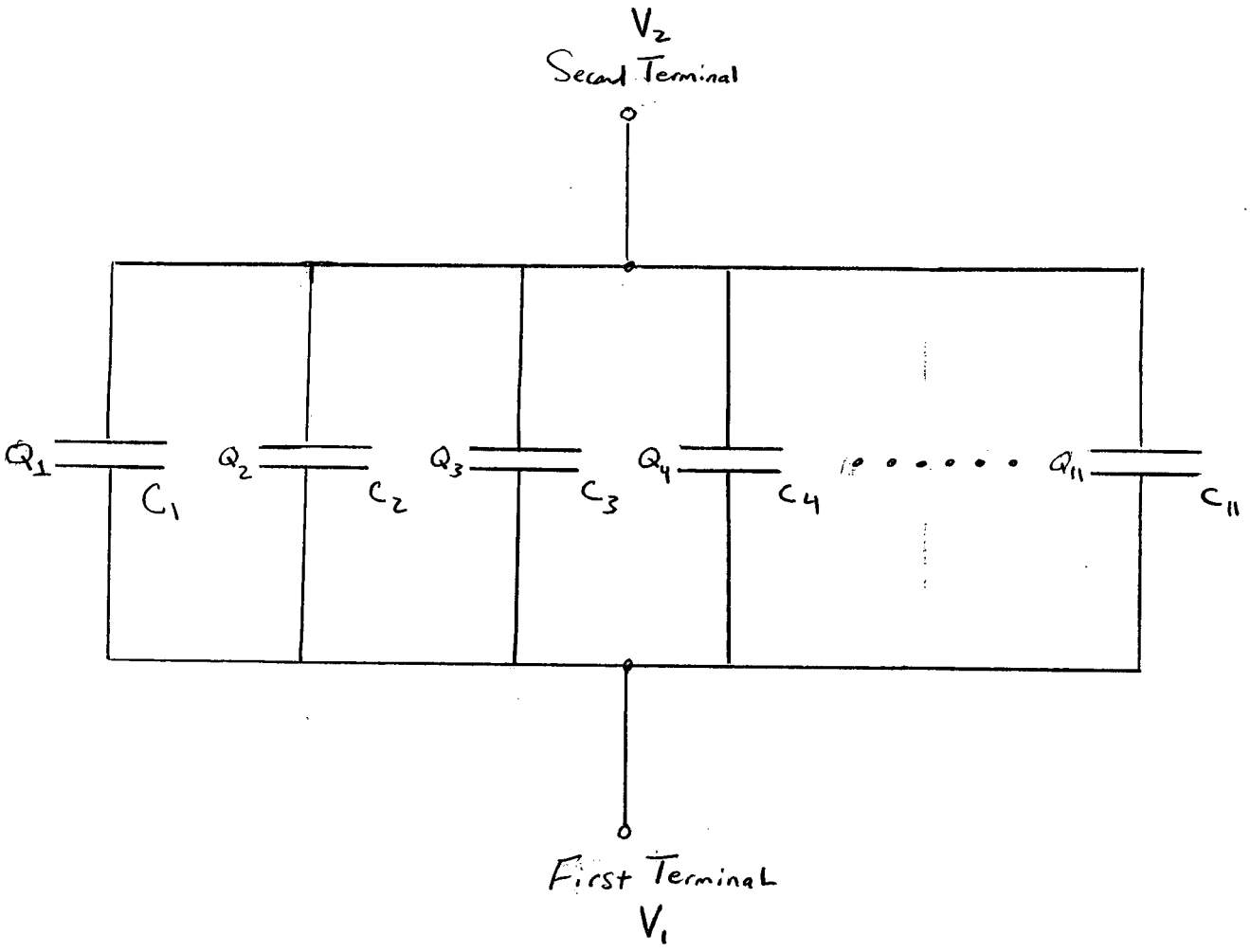
Fig. 1



$$Q_{Total} = Q_1 + Q_2 + Q_3 + Q_4 + Q_5 + Q_6 + Q_7 + Q_8 + Q_9 + Q_{10} + Q_{11}$$

Fig. 2

Fig. 3



$$Q = CV$$

$$C_{Total} = C_1 + C_2 + C_3 + \ldots + C_{11}$$

$$\Delta V = V_2 - V_1$$

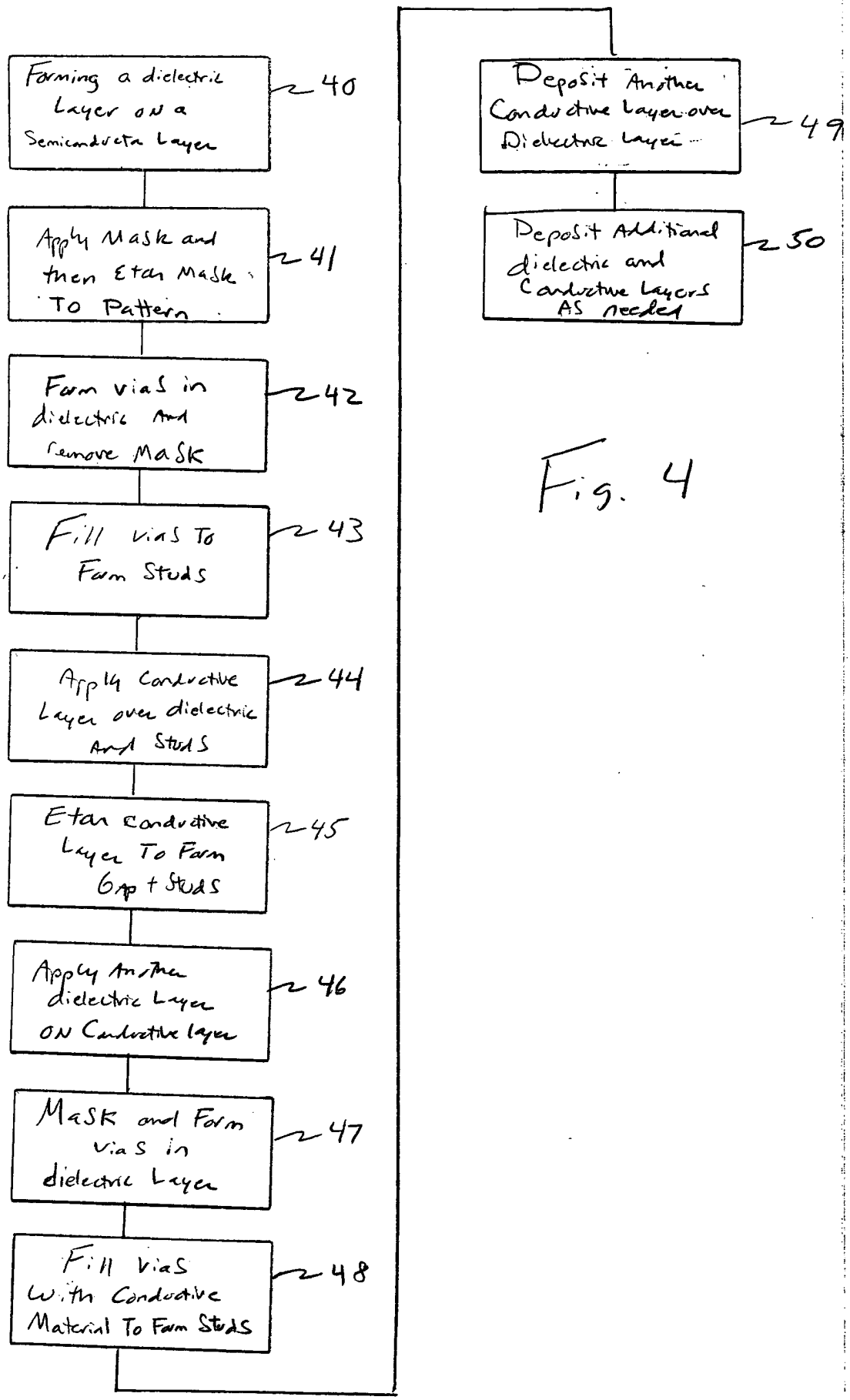

Forming a dielectric Layer on a Semiconductor Layer
40
Apply Mask and then Etch Mask To Pattern
41
Form vias in dielectric And remove MASK
42
Fill Vias To Form Studs
43
Apply Conductive Layer over dielectric And Studs
44
Etch Conductive Layer To Form Gap + Studs
45
Apply Another dielectric Layer ON Conductive layer
46
MASK and Form Vias in dielectric Layer
47
Fill Vias With Conductive Material To Form Studs
48
Deposit Another Conductive Layer over Dielectric Layer
49
Deposit Additional dielectric and Conductive Layers AS needed
50

Fig. 4

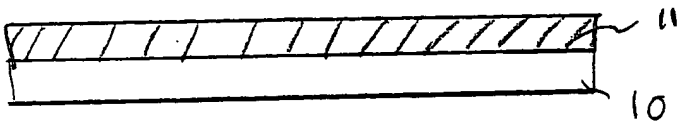


Fig. 5(a)

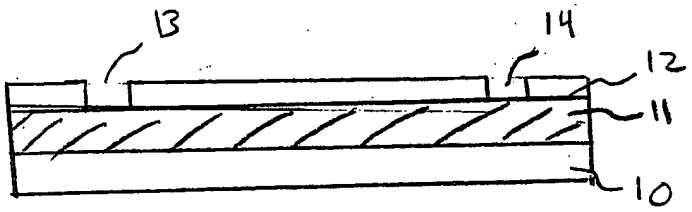


Fig. 5(b)

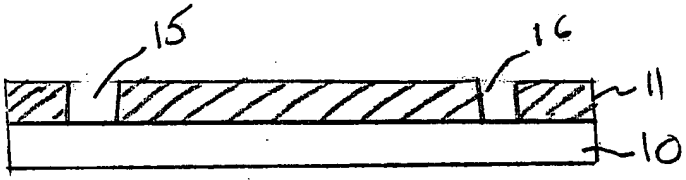


Fig. 5(c)

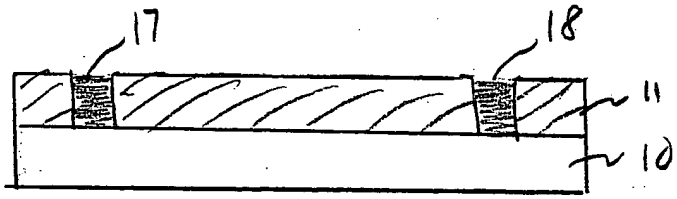


Fig. 5(d)

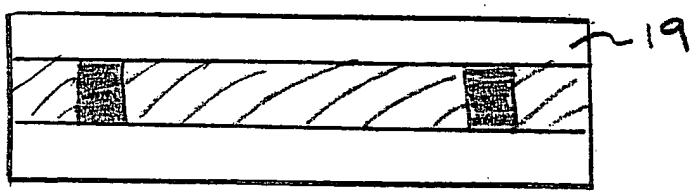


Fig. 5(e)

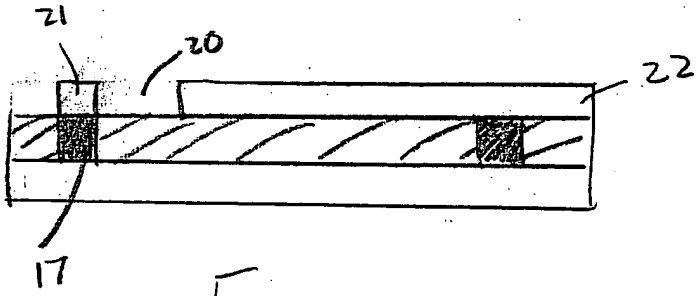


Fig. 5(f)

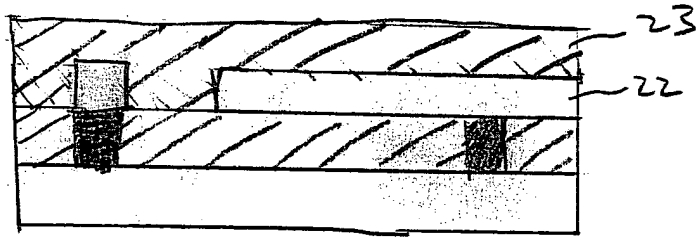


Fig. 5(g)

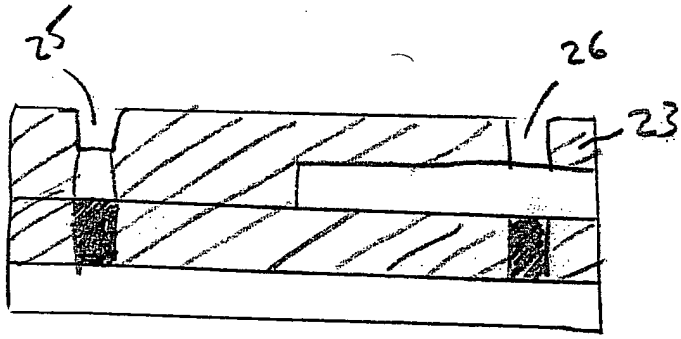


Fig. 5(h)

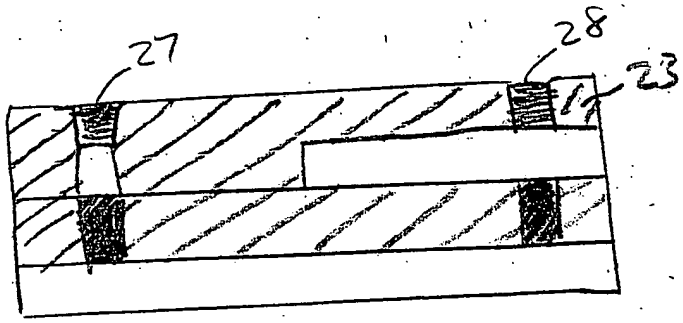


Fig. 5(i)

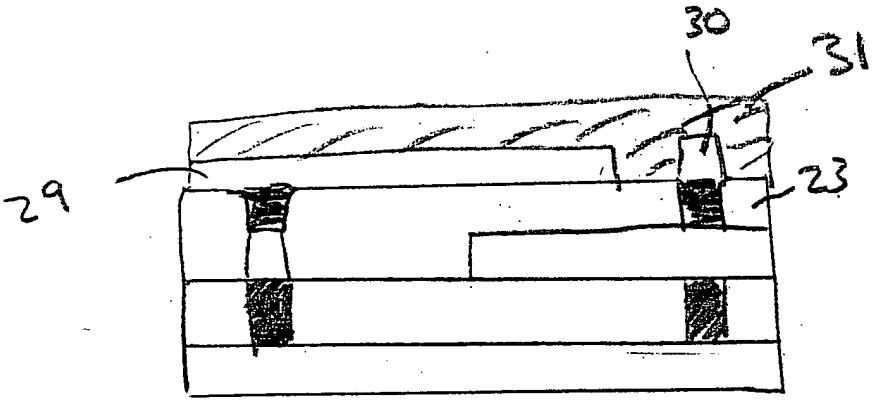


Fig. 5(j)

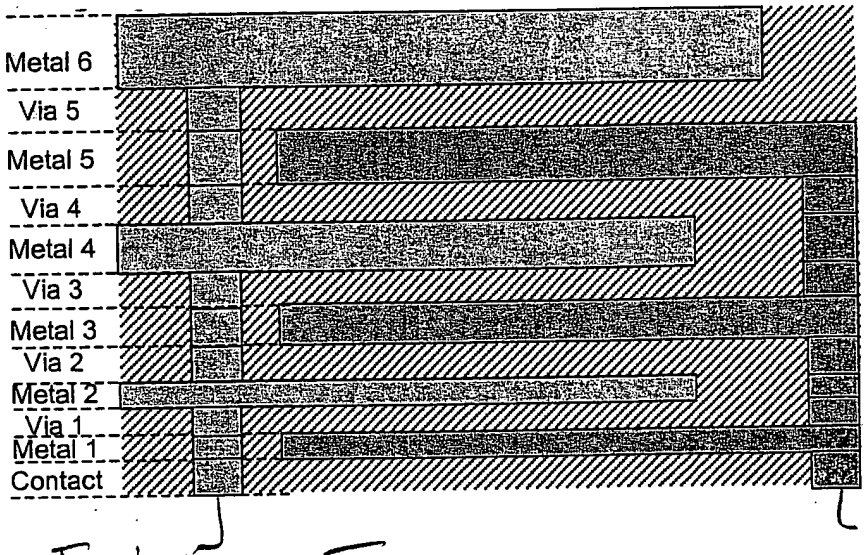


Fig. 5(k)

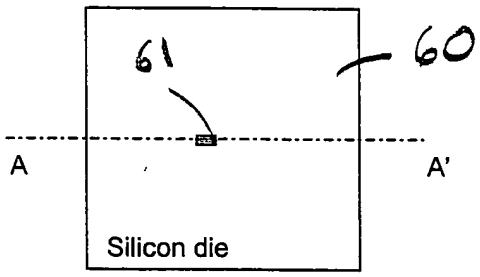


Fig.6(a)

Equivalent capacitor

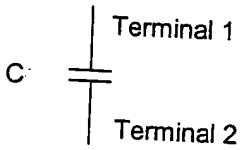


Fig.6(b)

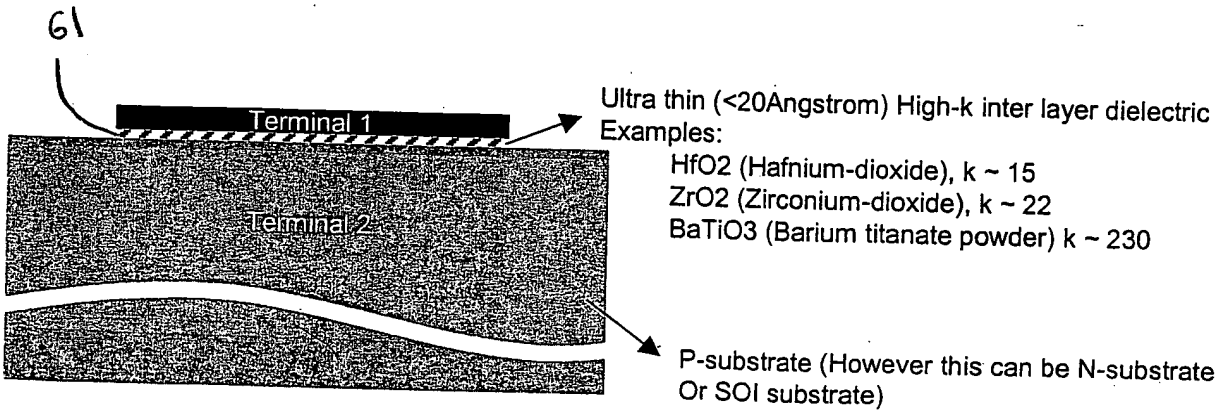


Fig. 6(c)

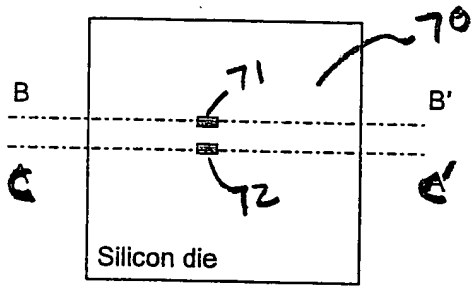


Fig. 7(a)

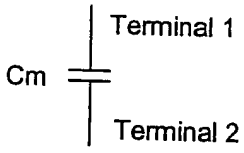


Fig. 7(b)

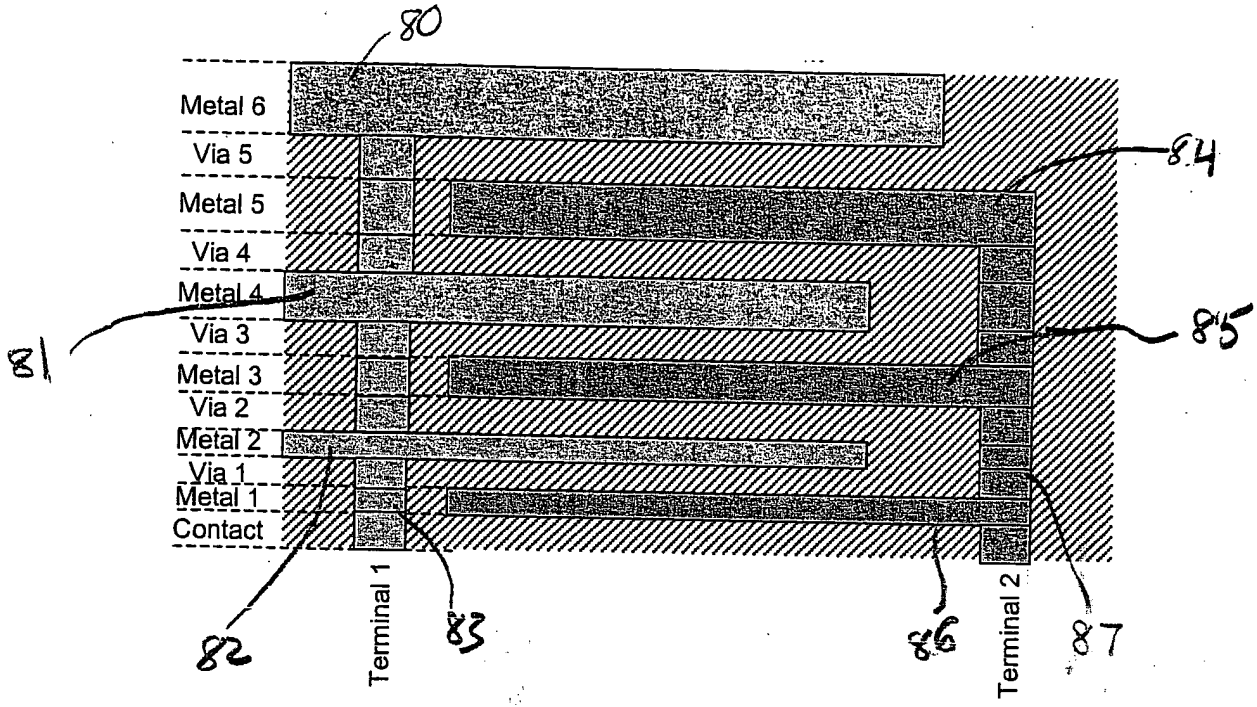

80
Metal 6
Via 5
Metal 5
Via 4
Metal 4
Via 3
Metal 3
Via 2
Metal 2
Via 1
Metal 1
Contact
81
82
Terminal 1
83
84
85
86
Terminal 2
87

Fig. 8(a)

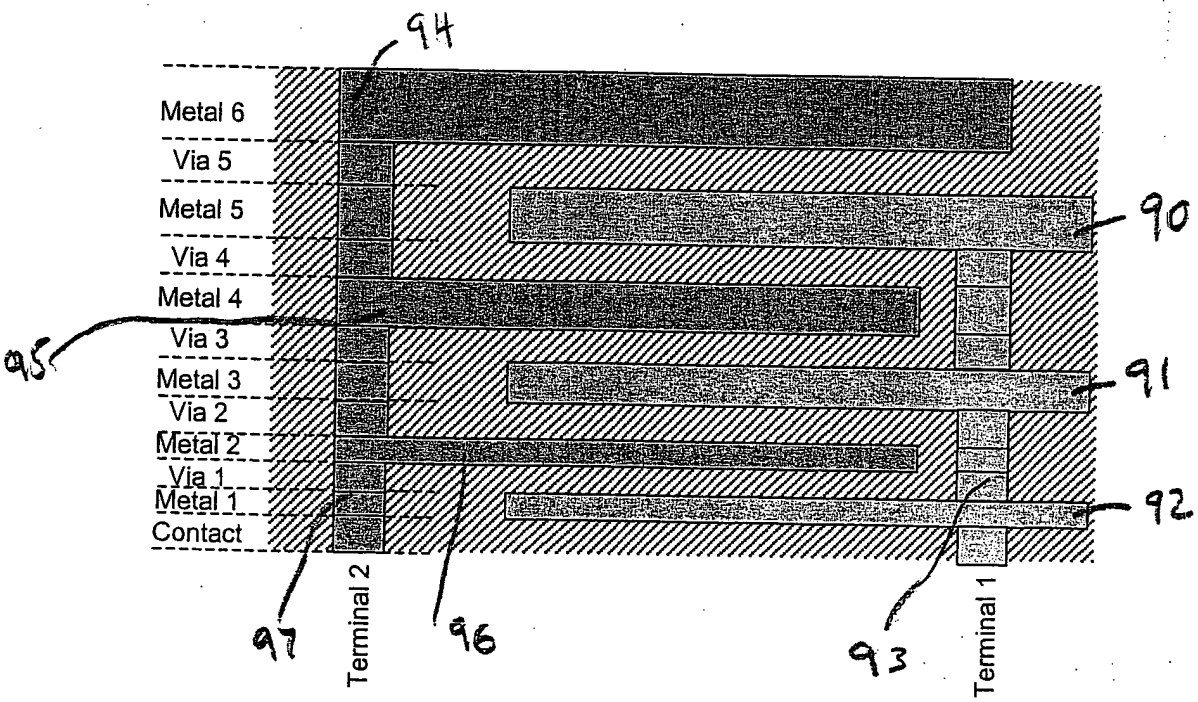

94
Metal 6
Via 5
Metal 5
Via 4
Metal 4
Via 3
Metal 3
Via 2
Metal 2
Via 1
Metal 1
Contact
95
90
91
92
97
Terminal 2
96
93
Terminal 1

Fig. 8(b)

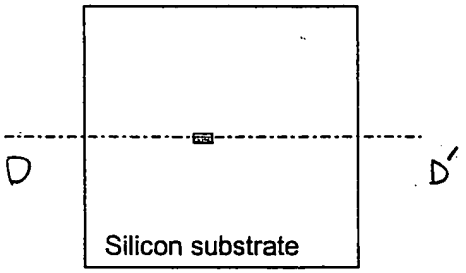


Fig. 9(a)

Equivalent capacitor

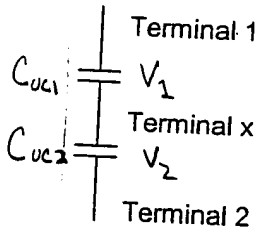


Fig. 9(b)

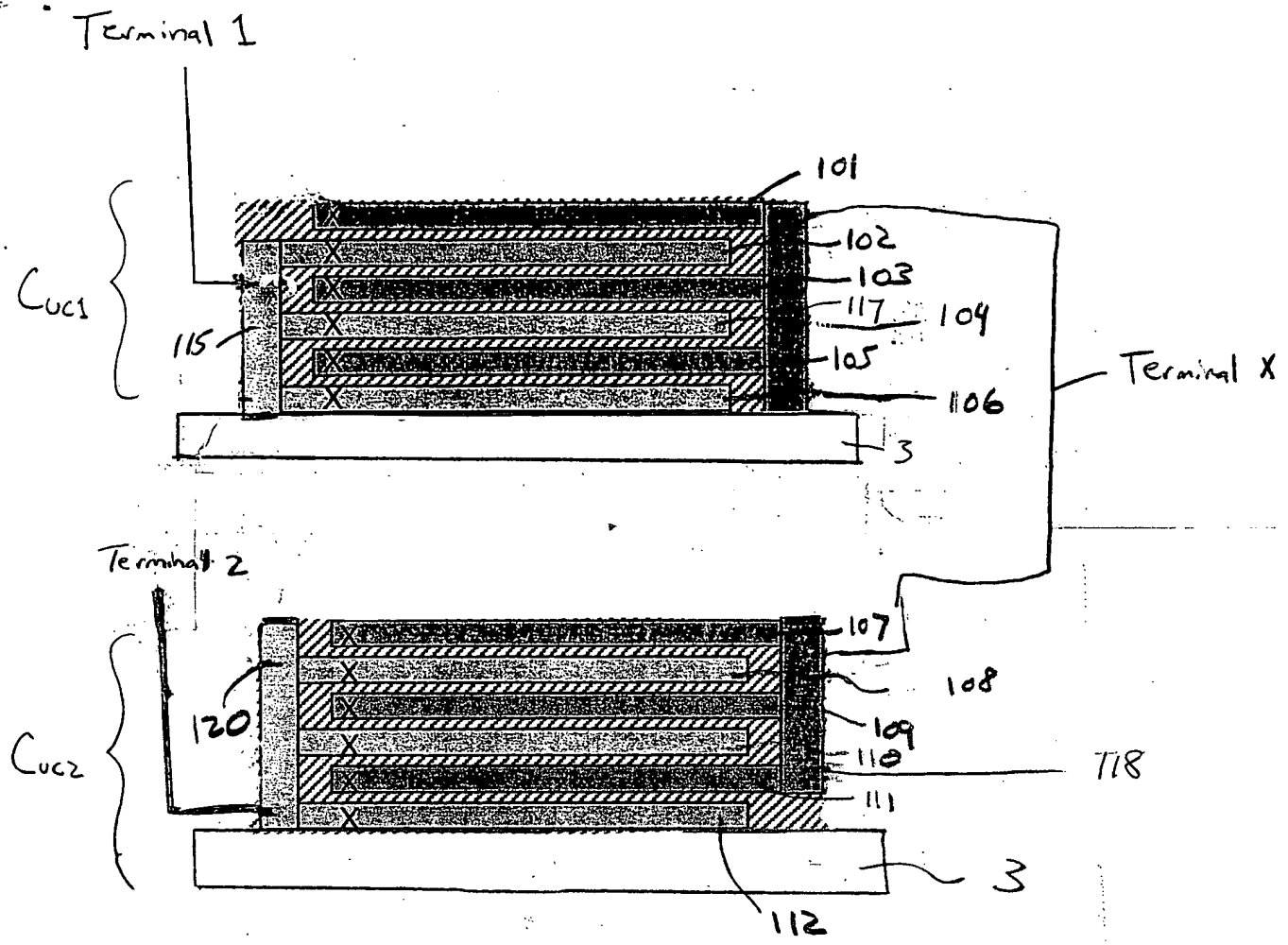
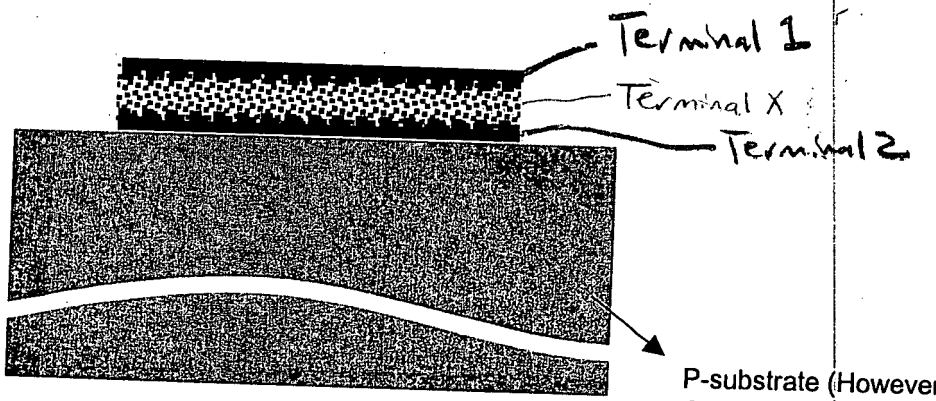

Terminal 1
101
102
103
117
104
105
106
Terminal X
C_{UC1}
115
3
Terminal 2
107
108
109
110
118
111
120
C_{UC2}
3
112

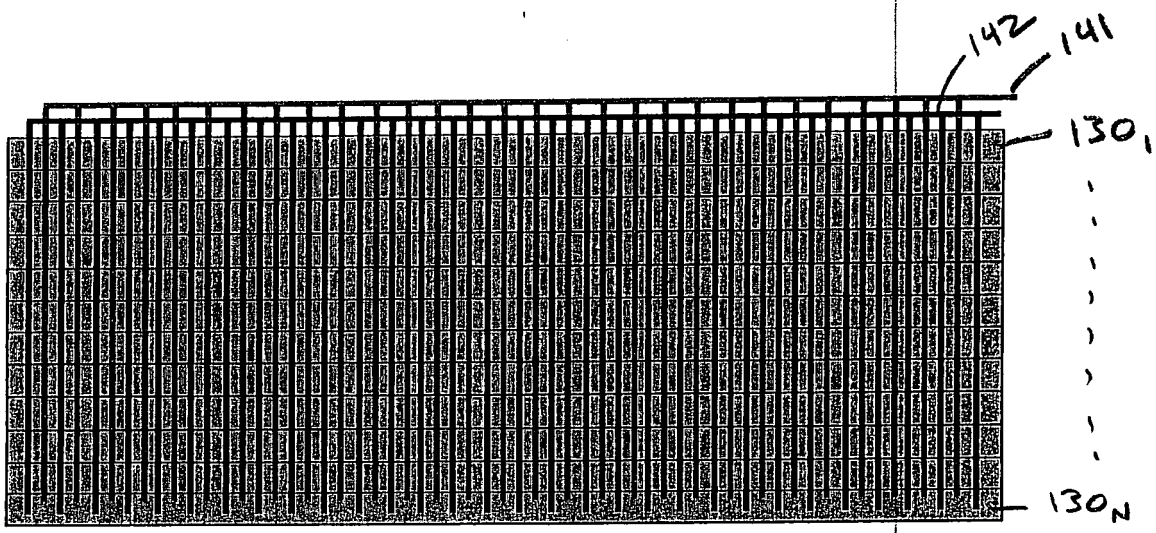
Fig. 10



Electrode (Terminal 1) – Example: Porous carbon or doped silicon. Can be conductive carbon or silicon nanotube.
Electrolyte (Terminal x) – Example: Potassium hydroxide
Electrode (Terminal 2) – Example: Porous carbon or doped silicon. Can be conductive carbon or silicon nanotube.

Fig. 11

Example cross section showing stacking of multiple substrate to increase the capacitance per unit area



Terminal 1
Terminal 2

Fig. 12

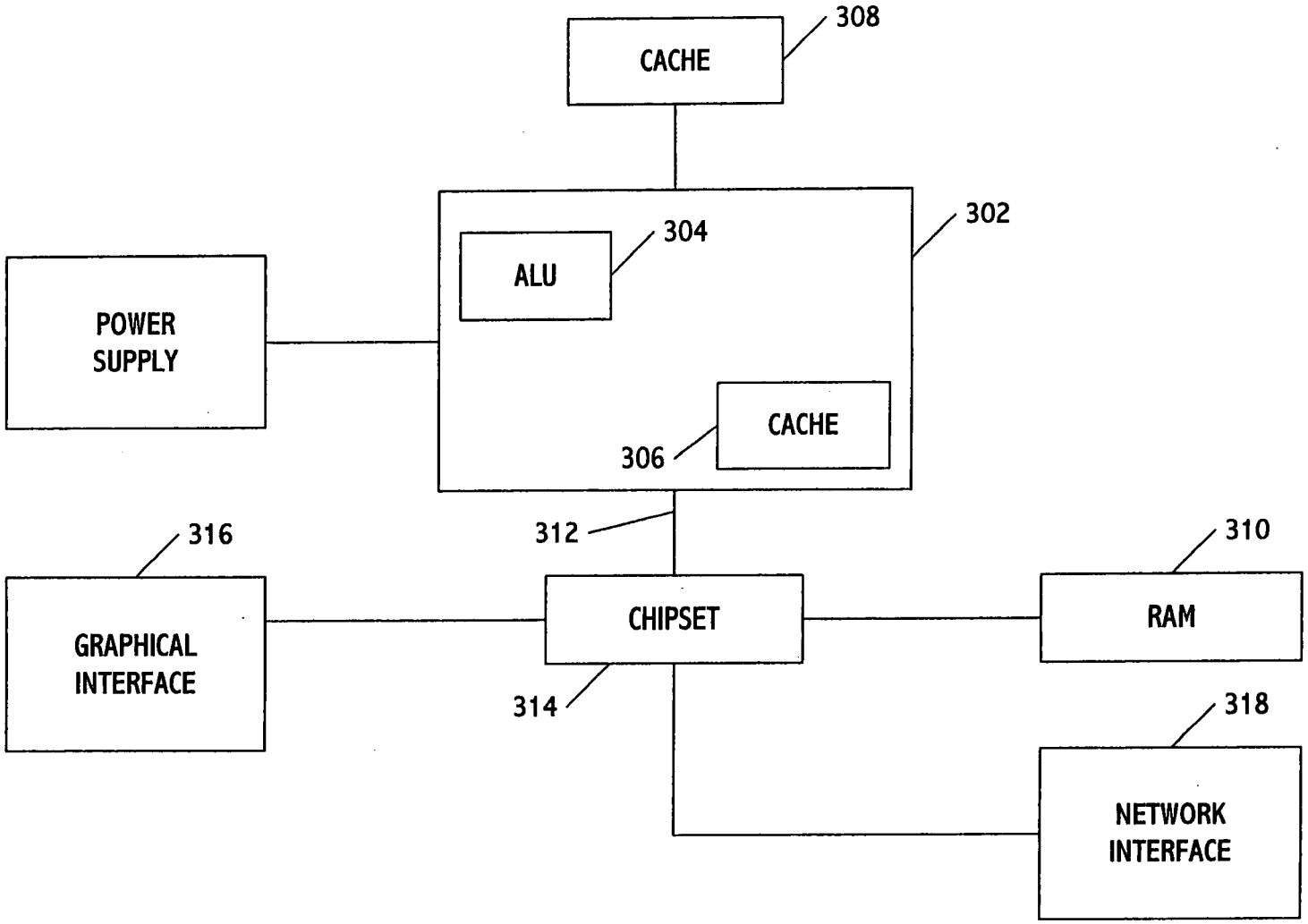

CACHE
308
302
ALU
304
POWER SUPPLY
CACHE
306
316
312
310
GRAPHICAL INTERFACE
CHIPSET
RAM
314
318
NETWORK INTERFACE

FIG.13